Features

Advanced Information

- 128-macrocell general purpose MAX EPLD optimized for designs requiring large amounts of buried logic
- 256 shareable expander product terms providing flexible logic expansion
  - over 32 product terms in a single macrocell
  - 128 additional latches provided by cross-coupling expanders
- Highest density 44 J-lead programmable logic device available; easily integrates over 60 TTL MSI and SSI components while consuming only 1/2 square inch of valuable board space
- Multiple-LAB MAX architecture with combinatorial decodes as fast as 25 ns, counter frequencies of 50 MHz, and pipelined data rates of 62 MHz
- Programmable I/O architecture allowing up to 36 inputs and 28 outputs
- 44-pin J-leaded, ceramic windowed or one-time-programmable plastic packages

General Description

The Altera EPM5127 is a user-configurable, high-performance MAX EPLD optimized for designs with large amounts of buried logic. For example, high-density serial communication subsystems and 8-bit data path functions can be quickly integrated into an EPM5127. The EPM5127 is a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic and 74HC logic. For example, a 74151 8-to-1 multiplexer consumes less than 1% of an EPM5127. In addition, it can integrate multiple 20- and 24-pin low-density PLDs.

The EPM5127, shown in Figure 13, consists of 128 macrocells equally divided into 8 Logic Array Blocks, each containing 16 macrocells. Each LAB also contains 32 expander product terms. The compact size of the LABs ensures high speeds, thus allowing better system performance.

The EPM5127 has 8 dedicated input pins, one of which may be used as a synchronous system clock. The device has 28 I/O pins that can be configured for input, output, or bidirectional data flow. These I/O pins feature dual feedback so that any macrocell can be buried while the I/O pin is being used as an input. Four of the LABs have 4 I/O pins, and 4 of the LABs have 3 I/O pins.

Figure 13. EPM5127 Block Diagram *The EPM5127 has 128 macrocells divided into 8 Logic Array Blocks. Note: Parentheses indicate J-leaded package pin numbers.*